## Abstract

The present invention comprises a dual bank FIFO memory buffer operable to buffer read data from memory and thereby compensate for specific timing problems in certain computerized systems. One embodiment of the invention includes a dual bank FIFO that comprises a first bank of memory elements operable to buffer memory data and a second bank of memory elements operable to buffer memory data. Write control address logic is operable to store selected memory data in memory elements with selected addresses within a bank of memory elements, and write control timing logic is operable to selectively grant write access to the banks of memory elements at predetermined time. Also, read control logic operable to read data stored in the first and second banks.

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